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TITLE: A METHOD AND APPARATUS FOR CALIBRATING A GM CELL UTILIZING A REPLICA GM CELL

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# A METHOD AND APPARATUS FOR CALIBRATING A GM CELL UTILIZING A REPLICA GM CELL

## BACKGROUND

**[0001]** A generalized biquad with a programmable boost and natural frequency is often used in continuous time filter applications. In particular, read/write channels for hard drives utilize integrated continuous time filtering on CMOS circuits. The stability of the cut-off frequency and boost of continuous time filters are among characteristics of an integrated filter. One popular method of constructing a generalized biquad is through the use of a Gm-C technique often used for signal processing applications in disk-drive read channels. CMOS Gm-C filters are useful for circuits involving high-frequencies.

**[0002]** The Gm-C technique allows for an in-circuit filter tuning with high speed and low power requirements. Typically, the transconductance is held constant while the capacitance is tuned in the circuit or the capacitance is held constant, while the transconductance is tuned. Often transconductance tuning is preferred due to a larger dynamic range and low distortion. By utilizing transconductance tuning, the corner frequency, $f_c$, and the gain, $Q$, of the filter can be obtained solely by modifying the transconductance, $Gm$, of Gm cells in the circuit.

**[0003]** The transconductance is often modified by adjusting a tuning voltage and/or tail current. Transconductance is defined by the following equation:

Eq. 1: $$Gm = \frac{I}{V},$$

where V is the input voltage and I is the output current of the Gm cell.

**[0004]** With NMOS transistors as Gm setting devices and the tail current held constant, the transconductance increases as the tuning voltage is increased. Similarly, the transconductance decreases as tuning voltage is decreased. For NMOS with the voltage held constant, the transconductance increases as the tail current is increases and the transconductance decreases as the tail current decreases.

**[0005]** Operation of a biquad, or other circuit in which Gm cells are utilized, is also affected by environmental factors, such as temperature, and manufacturing process tolerances. In order to account for these factors, proportional-to-absolute temperature current sources (PTAT sources) are often used. With PTAT techniques, a thermometer is embedded in a chip and the current sent to the Gm setting device(s) is delivered with respect to absolute temperature, i.e. a Kelvin based measurement, thereby adjusting the transconductance. This solution is problematic because the temperature dependency of the transconductance is not necessarily linear. Moreover, an exact mathematical representation of the effect of temperature on the transconductance is often not known.

**[0006]** The PTAT approach suffers from large variations against changes of environmental temperature and often requires an increase in a power supply voltage above the safe upper limit of the process. Additionally, the circuit is sensitive to noise in the substrate or other circuits.

## SUMMARY

**[0007]** Tunable Gm cells may be used to provide filtering and gain adjustments. Often these tunable Gm cells are used in a biquad, a second order filter. The transfer function is dependent on the transconductance (Gm) of the tunable Gm cells. Gm cells are often tuned by adjusting a tuning voltage. This process is known as tuning.

**[0008]** Replica cells can calibrate the Gm cells by providing the Gm cells with the correct tuning voltage. Additionally, the replica cells may be used to provide the Gm cells with a bias voltage.

**[0009]** In one aspect, a Gm replica cell is operable to receive a Gm setting code and provide a tuning voltage to a Gm cell. Here, the tuning voltage is adjusted until the difference between two drain currents passing through the input transistors are equal to a current reference. When this relationship is achieved the transconductance of the replica cell, and the Gm cell to which it is connected, is equal to the positive output current reference divided by the difference between

the high voltage reference and a low voltage reference. Under these conditions, the transconductance of the cell is calibrated.

**[0010]** The features of the preferred embodiments of the present invention are further described in the detailed description section below.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0011]** Figure 1 depicts a circuit diagram for one embodiment of a Gm replica cell.

**[0012]** Figure 2 depicts a circuit diagram for another embodiment of a Gm replica cell.

**[0013]** Figure 3 depicts one embodiment of generalized biquad stage that utilizes Gm replica cells.

**[0014]** Figure 4 depicts one embodiment of a circuit for a multiplying current output digital to analog converter.

**[0015]** Figure 5 depicts one embodiment of a circuit for a stable reference current generator.

**[0016]** Figure 6 depicts one embodiment of a circuit for a common mode feedback circuit.

## DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

**[0017]** The embodiments described herein relate to a method and apparatus for calibrating a Gm cell utilizing a replica Gm cell. Herein, the phrase "connected with" is defined to mean directly connected to or indirectly connected with through one or more intermediate components. Such intermediate components may include both hardware and software based components. The present application has been filed currently with U.S. Patent Application Serial Number 09/865,863, now U.S. Patent 6,420,064, filed on May 25, 2001, assigned attorney docket number 01 P 09240 US and titled, "METHOD AND APPARATUS FOR AN EFFICIENT LOW

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VOLTAGE SWITCHABLE GM CELL," the entire disclosure of which is incorporated herein by reference.

**[0018]** The preferred embodiments of the present invention may be designed for use with either a conventional Gm cell, a Gm cell disclosed in the above referenced co-pending application, or other Gm cells. A replica cell substantially matches the electrical properties of the Gm cell that it calibrates. In particular, the Gm setting devices and the input transistors of the replica cell are matched with those of the Gm cell. Further, if used, cascode transistors connected with the input transistors may also be matched. A replica scenario also exists if the tail current and the channel width of the transistors in the signal path are scaled with the same factor. For example, the channel width of the transistors in the replica cell may be one-quarter of the channel width of the transistors of the Gm cells in the signal path if the tail current of the replica Gm cell is one-quarter of the tail current of the Gm cells in the signal path. In this example, the pull-up current sources need not match.

**[0019]** Figure 1 depicts a circuit diagram for a replica cell designed for use the switchable Gm cell of U.S. Patent Application Serial Number 09-865,863, filed on May 25, 2001, now U.S. Patent 6,480,064 assigned attorney docket number 01 P 09240 US and titled, "METHOD AND APPARATUS FOR AN EFFICIENT LOW VOLTAGE SWITCHABLE GM CELL." Figure 2 depicts a circuit diagram for a replica cell designed for use with a conventional Gm cell. Where the elements described are the same, like numbers have been utilized.

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**[0020]** In Figure 1, a current multiplying digital-to-analog converter **100** with differential current output is provided. The digital-to-analog converter **100** has inputs for a Gm setting code **105** and connects with a positive supply voltage **110** and a reference current **115**. The digital-to-analog converter **100** has outputs for positive current **120** and negative current **125**. The digital-to-analog converter **100** generates a stable current, $I_{dac1}$, that is proportional to the value of the digital code received by the Gm setting code input **105** and the reference current **115**.

**[0021]** An exemplary multiplying current output digital-to-analog converter **400** is depicted in Figure 4. An exemplary circuit for the generation of a highly

accurate and stable reference current using an external reference resistor with only one chip-pin is depicted in Figure 5. Other circuit designs may also be used. For example, the circuit of Figure 4 may be implemented with internal reference resistors.

**[0022]** Referring back to Figure 1, positive current output **120** is connected with the drain and gates of a current mirror first transistor **130**, the gate of a current mirror second transistor **135**, and the gate of a tail current transistor **140**. Current mirror first transistor **130** and current mirror second transistor **135** operate as a current mirror in which $I_{dac1} = I_{dac2}$. In another embodiment, $I_{dac2}$ may also be designed to be an arbitrary multiple of $I_{dac1}$. This may be accomplished by altering the ratio of channel widths of the transistors **130** and **135**.

**[0023]** The tail current transistor **140**, in conjunction with current mirror first transistor **130**, also operates as a current mirror and generates $I_{tail}$. In a preferred embodiment, the tail current transistor **140** is constructed with a channel width that is greater than the channel width of the current mirror first transistor **135** or the current mirror second transistor **140**. The channel width is a matter of design preference. In Figure 1, channel width $w_2$, is greater than channel width $w_1$ because there are more devices driven by the tail current.

**[0024]** In the embodiment of Figure 1, the Gm setting code **105** consists of bits of a binary word. In an embodiment for use with the switchable Gm cell disclosed in U.S. Patent Application Serial Number 09-865,863, filed on May 25, 2001, now U.S. Patent 6,480,064, assigned attorney docket number 01 P 09240 US and titled, "METHOD AND APPARATUS FOR AN EFFICIENT LOW VOLTAGE SWITCHABLE GM CELL," the Gm setting code **105** also determines which of the Gm setting devices **145** (shown here in a binary coding arrangement) are turned on. Because the tail current, $I_{tail}$, is dependent on $I_{dac1}$, which is dependent on the Gm setting code **105**, the voltage drop across the Gm setting devices **145** will remain constant. For example, if an original Gm setting code of 3 is doubled to 6, $I_{dac1}$ and $I_{tail}$ both double. At the same time, the switching circuit **150** (shown here without a decoding circuit) receives the Gm setting code **105** and will turn on the appropriate Gm setting devices in order to double the overall transconductance of

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the Gm setting devices **145**. In this example, where Gm setting devices 1 and 2 were formerly turned on for a code of 3, the change to 6 results in Gm setting devices 2 and 3 turned on and the rest turned off. Here, the transconductance of the Gm setting devices, as a whole, doubles at the same time as the doubling of the tail current. Consequently, the voltage drop across the Gm setting devices remains constant. Thus, the operation of the rest of the replica cell is not affected and the process of determining a proper tuning voltage is enhanced. In other embodiments, such as the embodiment shown in Figure 2, the tuning voltage accounts for the change in the transconductance of the Gm cell. In another embodiment, the tail current may be held constant. Here, the voltage drop across the Gm setting devices will change by reducing the Gm.

**[0025]** The Gm setting devices **145** are connected with a first input transistor **155** and a second input transistor **160**. The first input transistor **155** is connected with a high reference voltage. The second input transistor **160** is connected with a low reference voltage. Since the values of these two voltages are not the same, currents $I_1$ and $I_2$ will have different magnitudes. The input transistors **155** and **160** are connected with cascode transistors **165** and **170**. Cascode transistors **165** and **170** are connected with cascode transistors **175** and **180**. Cascode transistors **175** and **180** are connected with a mirrored pull-up current source **185** and a mirror reference transistor **190**.

**[0026]** The gates of the mirrored pull-up current source **185** and a mirror reference transistor **190** are connected with the drain of current mirror second transistor **135**, the drain of the cascode transistor **180**, the drain of the cascode transistor **170**, and the positive input of the error amplifier **195**. The drains of the cascode transistors **165** and **175** are respectively connected with the two inputs of an error amplifier **195**. The mirrored pull-up current source **185**, mirror reference transistor **190**, and casode transistors **175** and **180** comprise a current mirror that configures the replica cell as a single-ended amplifier, instead of a differential amplifier.

**[0027]** One input of the error amplifier **195** is connected with the drain of the cascode transistor **175** and the other is connected with the drain of cascode

transistor **180.** The error amplifier **195** outputs the difference between the drain voltages, $V_1$ and $V_2$, multiplied by a gain, and supplies a tuning voltage to the Gm setting devices. The gain utilized by the error amplifier **195** is often in the range of 20dB and 100dB. Numerous different circuit designs for the operation of the error amplifier **195** may be used.

**[0028]** The replica cell insures that the transconductance, Gm, is equal to the positive output current, $I_{dac1}$, divided by the difference between the high reference voltage, $V_{refH}$, and the low reference voltage, $V_{refL}$. Thus, the following relationship is desired:

Eq. 2: $$Gm = \frac{I_{dac1}}{V_{refH} - V_{refL}}$$

If this equation is satisfied, the transconductance of the GM cell is properly set. The error amplifier **195**, in accordance with the design of the replica cell, adjusts the tuning voltage until this condition is met.

**[0029]** Because the current mirror first transistor **130** and current mirror second transistor **135** have the same characteristics, namely substantially the same channel width and channel length,

Eq. 3: $$I_{dac1} = I_{dac2}$$

Similarly, because of the difference in the channel width between tail current source **140** and the current mirror first transistor **130**,

Eq. 4: $$I_{tail} = \left(\frac{w_2}{w_1}\right) I_{dac1}$$

Additionally, under ideal circumstances, the following equations are applicable:

Eq. 5: $$I_3 = I_{dac2} + I_2$$

Eq. 6: $$I_4 = I_3$$

Eq. 7: $$I_1 - I_2 = (V_{refH} - V_{refL})Gm$$

Eq. 8: $$I_1 = I_4$$

By combining equations 5, 6, and 8, the following equation results:

Eq. 9: $$I_1 - I_2 = I_{dac2}$$

Equation 9 represents the condition in which the Gm cell is properly tuned. If $I_1 - I_2 < I_{dac2}$, the transconductance, Gm, of the Gm cell is too low. Under this condition, error amplifier **195** yields a lower tuning voltage. Similarly, if $I_1 - I_2 > I_{dac2}$, the transconductance of the Gm cell is too high. Here, the error amplifier **195** yields a higher tuning voltage.

**[0030]** In the preferred embodiment of Figure 1, the following dimensions may be utilized:

Positive Output Current $\mathbf{I_{dac1}}$: Gm Setting * 2.5 uA
Current Mirror First and Second Transistors **130**, **135**: W=36μm, L=0.36μm
Tail current source **140**: W=36μm, L=0.36μm
Gm Setting Devices **145**: W=0.4μm, L=0.4μm
Input transistors **155**, **160**: W=100μm, L=0.18μm
NMOS cascode transistors **165**, **170** : W=100μm, L=0.18μm
PMOS cascode transistors **175**, **180**: W=360μm, L=0.18μm
Mirror Pull-up Current Source **185**: W=36μm, L=0.36μm
Mirror Reference Transistor **190**: W=36μm, L=0.36μm

**[0031]** For certain applications, it may also be desirable to use a higher resolution in the digital-to-analog converter. For example, another embodiment of the replica cell may be accomplished by using a 10-bit Gm setting code **105**. At the same time, this embodiment may continue to use six pairs of Gm setting

devices and six Gm setting controls. Here, the first six most significant bits of the digital-to-analog converter **100** are connected to the six Gm setting controls. The remaining 4 least significant bits may be used to change the positive output current, $I_{dac1}$. By adjusting the output current, variations in manufacturing process, temperature, and power supply voltage may be additionally compensated by the digital-to-analog converter **100**.

**[0032]** Referring now to Figure 2, this embodiment is designed for use with a conventional Gm cell. In this embodiment, the Gm setting controls **150** are not utilized.

**[0033]** In Figure 2, a current multiplying digital-to-analog converter **100** with differential current output is provided. The digital-to-analog converter **100** has inputs for a Gm setting code **105** and connects with a positive supply voltage **110** and a reference current **115**. The digital-to-analog converter **100** has outputs for positive current **120** and negative current **125**. The digital-to-analog converter **100** generates a stable current, $I_{dac1}$, that is proportional to the value of the digital code received by the Gm setting code input **105** and the reference current **115**.

**[0034]** A positive current output **120** is connected with the drain and gates of a current mirror first transistor **130**, the gate of a current mirror second transistor **135**, and the gate of a tail current transistor **140**. Current mirror second transistor **135** generates $I_{dac2}$. The tail current transistor **140** generates $I_{tail}$.

**[0035]** The Gm setting devices **200** are connected with a first input transistor **155** and a second input transistor **160**. The first input transistor **155** is connected with a high reference voltage. The second input transistor **160** is connected with a low reference voltage. The input transistors **155** and **160** are connected with cascode transistors **165** and **170**. Cascode transistors **165** and **170** are connected with cascode transistors **175** and **180**. Cascode transistors **175** and **180** are connected with a mirrored pull-up current source **185** and a mirror reference transistor **190**.

**[0036]** The gates of the mirrored pull-up current source **185** and a mirror reference transistor **190** are connected with the drain of current mirror second transistor **135**, the drain of the cascode transistor **180**, the drain of the cascode

transistor **170**, and the positive input of the error amplifier **195**. The drains of the cascode transistors **165** and **175** are respectively connected with the two inputs of an error amplifier **195**.

**[0037]** One input of the error amplifier **195** is connected with the drain of the cascode transistor **175** and the other is connected with the drain of cascode transistor **180.** The error amplifier **195** outputs the difference between the drain voltages, $V_1$ and $V_2$, multiplied by a gain, and supplies a tuning voltage to the Gm setting devices. As one of ordinary skill in the art would recognize, numerous types of Gm cells and Gm setting devices may be utilized in accordance with the present invention.

**[0038]** Further, the Gm replica cells depicted in Figure 1 and 2 may also be modified in accordance with the present invention. For example, instead of utilizing a current mirror comprised of the mirrored pull-up current source **185**, mirror reference transistor **190**, and casode transistors **175** and **180**, a common mode feedback loop may be utilized. An example of a common mode feeback loop is depicted in Figure 8 of U.S. Patent Application Serial Number 09-865,863, filed on May 25, 2001, now U.S. Patent 6,480,064, assigned attorney docket number 01 P 09240 US and titled, "METHOD AND APPARATUS FOR AN EFFICIENT LOW VOLTAGE SWITCHABLE GM CELL," by the arrangement of current sources **102** and **104**, cascode transistors **106** and **108**, and error amplifier **830**. A similar arrangement may be used in a replica Gm cell.

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**[0039]** The replica Gm cell may be used in a variety of applications. Figure 3 depicts an embodiment in which a generalized biquad stage has a digitally programmable boost (Q) and natural frequency (fc) that uses 6 bit binary digital codes. In this embodiment, a pair of Gm replica cells are used to calibrate the Gm cells **320, 330** that implement a second order filter represented by the following transfer function:

Eq. 10:
$$H(s) = \frac{1}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}}$$

where natural frequency $\omega_0 = \frac{Gm_1}{C} = f_c \frac{Gm_u}{C}$ and peaking factor $Q = \frac{Gm_1}{Gm_2} = \frac{f_c}{Q_c}$, and $f_c$ and $Q_c$ are binary coded digital numbers.

**[0040]** In this embodiment, there are three $Gm_1$ cells **300** and one $Gm_2$ cell **310**. Gm1 replica cell **320** and Gm replica cell **330** are used to calibrate the Gm1 cells **300** and Gm2 cell **310** respectively. The Gm replica cells **320** and **330** supply the Gm cells **300** and **310** with a tuning voltage and a bias voltage. In the circuit configuration of Figure 3, the altering of $Gm_1$ and $Gm_2$ may be used to adjust the natural frequency and/or the boost of the transfer function realized.

**[0041]** As one skilled in the art would appreciate, for operation in the signal path, several different types of Gm cells may be utilized. For example, Gm replica cells may be designed for use with the circuits depicted in Figures 1, 2, 8, 9, and 10 of U.S. Patent Application Serial No. U.S. Patent Application Serial Number 09-865,863, now U.S. Patent 6,480,064, filed on May 25, 2001, assigned attorney docket number 01 P 09240 US and titled, "METHOD AND APPARATUS FOR AN EFFICIENT LOW VOLTAGE SWITCHABLE GM CELL." Further, the replica Gm cells may incorporate the use of the Gm setting devices depicted in Figures 3 and 4 of U.S. Patent Application Serial No. U.S. Patent Application Serial Number 09-865,863, now U.S. Patent 6,480,064, filed on May 25, 2001, assigned attorney docket number 01 P 09240 US and titled, "METHOD AND APPARATUS FOR AN EFFICIENT LOW VOLTAGE SWITCHABLE GM CELL," conventional Gm setting devices, or other Gm setting devices.

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**[0042]** Additionally, in Figure 3, common mode feedback circuits **340** and **350** are connected with the $Gm_1$ cells **300** and $Gm_2$ cell **310** respectively to ensure that the proper pull-up current is provided to them and the common mode output voltage is stable. An exemplary circuit for a the common mode feedback circuits **340** and **350** is depicted in Figure 6.

**[0043]** It is to be understood that a wide range of changes and modifications to the embodiments described above will be apparent to those skilled in the art and are contemplated. It is therefore intended that the foregoing detailed description be regarded as illustrative, rather than limiting, and that it be understood that it is

the following claims, including all equivalents, that are intended to define the spirit and scope of the invention.